REMARKS

Claims 1-7, 9-27, and 29-32, and 40-43 were pending. No claims have been amended. No claims have been added or canceled. Accordingly, claims 1-7, 9-27, 29-32, and 40-43 remain pending subsequent entry of the present amendment.

Re: Examiner's Response to Arguments

In paragraph 44 of the present Office Action, it is suggested that the previously cited reference Motorola MCF5206 Integrated Microprocessor, as described in Freescale Semiconductor, Inc. Product Brief "MCF5206 Integrated Microprocessor" (hereinafter "MCF5206"), teaches external interrupts have architecturally fixed interrupt priorities. However, Applicant disagrees. First, architecturally fixed interrupt priorities are fixed by a system architecture. Architecturally fixed interrupt priorities are not configurable and are not programmable, especially by a user. Applicant submits this is the meaning one skilled in the art would give the term "architecturally fixed". Second, nowhere in the cited reference MCF5206 does it teach architecturally fixed interrupt priorities.

Concerning the first point, external interrupts having architecturally fixed interrupt priorities, which differ from priorities that are configurable, are features of the presently claimed invention. Such features are also described in the Specification:

> "That is, the inventor envisions that in one embodiment, the interrupts I0 through I7 should have their interrupt priority already defined (architecturally), while allowing the core interrupts to be configured as will be described further below with reference to FIG. 5." (Specification, paragraph 0040) (emphasis added)

Here, interrupts I0-I7 have architecturally fixed interrupt priorities. The user is not able to alter these priority values. However, the core interrupts are contrasted with the external interrupts and have priorities that are configurable. The core interrupt priorities are not fixed by the system architecture. The below excerpt from the Specification describes an example of how a user may configure the core interrupt priorities, which are not architecturally fixed, to have intermittent values with the architecturally fixed priorities of interrupts I0-I7.

> "For example, presume that interrupts I0-I7 have architected priorities of levels 1, 2, 3, 4, 5, 6, 7, and 8, respectively. Presume further that interrupts I8 and I9 have been programmed to have a priority level of 4.5, that interrupt I10 has a programmed priority level of 1.5, and that interrupt I11 has a programmed priority level of 0.5. Then, the encoder 440 would prioritize the received interrupts in the following order:
>
> 1 Priority Interrupt Level I11 0.5 I0 1.0 I10 1.5 I1 2.0 I2 3.0 I3 4.0 I8, I9 4.5 I4 5.0 I5 6.0 I6 7.0 I7 8.0" (Specification, paragraph 0049)
>
> "The present invention has thus allowed a system designer to configure an interrupt strategy for core produced interrupts without altering the interrupt priority architecture defined within an existing interrupt controller." (Specification, paragraph 0053) (emphasis added)

As can be seen above, interrupts I0-I7 have architecture-defined priorities within an interrupt controller of a computing system. These priorities are not configurable by the user.

In addition to the above, it appears this difference between architecturally fixed priorities and configurable priorities was also previously recognized by the examiner as shown below from the Office Action dated September 20, 2005, page 2, paragraph 4, wherein the examiner stated:

> "It is further unclear how an architecturally fixed interrupt priority can be established by an interrupt controller, as this requires some means for the interrupt priorities to be programmed by the interrupt controller, and thus are not architecturally fixed."

Therefore, in the earlier Office Action, the examiner acknowledged that interrupt priorities which can be programmed are (thus) not architecturally fixed.

Present claim 1 recites the following features:

> "a plurality of first interrupts generated by a core, said plurality of first interrupts having programmable priorities;
> a plurality of second interrupts that are generated external to said core, said second interrupts having architecturally fixed interrupt priorities." (emphasis added).

Applicant has reviewed the reference MCF5206 as in the previous response and submits this reference nowhere teaches these features. Paragraph 44 on page 18 of the present Office Action states:

> "Applicant has argued that none of the references disclose that the external interrupts have an architecturally fixed interrupt priority (See Pages 9-11). In response, the Examiner notes that only MCF5206 was relied upon to disclose this feature. MCF5206 discloses that the 3 external interrupts can be configured as fixed interrupt levels 1, 4, and 7. Interrupt levels 1, 4, and 7 are architecturally fixed, and thus the external interrupts have architecturally fixed interrupt priorities." (emphasis added)

The examiner has stated that the 3 external interrupts of MCF5206 can be configured. By being able to be configured, such as being programmed by a user which is disclosed by the reference as shown further below, the external interrupts are not architecturally fixed. The external interrupts cannot be both configurable

and architecturally fixed. The cited reference MCF5206 teaches the external interrupts are configurable by being programmed by a user. The citations that teach away from the features of claim 1 are provided in the following:

> "Programmable interrupt controller
> low interrupt latency
> 3 external interrupt inputs
> Programmable interrupt priority and autovector generator" (MCF5206, page 2). (emphasis added).

> "Interrupt Controller. The interrupt controller provides user-programmable control of 3 or 7 external interrupt and 5 internal peripheral interrupts. Users can program each internal interrupt to any one of 7 interrupt levels and 4 priority levels within each of these levels. The 3 external interrupt signals can be configured as either fixed interrupt levels 1, 4, and 7, or as a 7-level encoded interrupt. Users can program the external interrupts to any one of the 4 priority levels within the respective interrupt levels." (MCF5206, page 5). (emphasis added).

For at least the above reasons, claim 1 is patentably distinct from the cited reference.

Also in the present Office Action, paragraph 45 on page 18, it is suggested that it is inherent that the reference MCF5206 will have a priority encoder as recited in claim 1. However, Applicant disagrees. Claim 1 recites:

> "a priority encoder, coupled to both said first interrupts and to said second interrupts, and to said status register, said priority encoder prioritizing said first and second pluralities of interrupts utilizing said programmable priorities for said first interrupts and said architecturally fixed interrupt priorities for said second interrupts." (emphasis added)

As seen from the above, a priority encoder is recited which prioritizes programmable and architecturally fixed interrupt priorities. As already noted, the cited art does not disclose the architecturally fixed priorities as recited. Therefore, such a priority encoder is neither disclosed, inherent, nor suggested by the reference. In contrast, the reference may simply suggest a priority encoder for encoding programmable interrupt priorities. For at least these further reasons, claim 1 is patently distinguishable from the cited art.

For purposes of economy, Applicant's comments in the previous Response are repeated and are incorporated herein by reference.

In view of the above, Applicant submits the claims are patentably distinct from the combination of cited art. Accordingly, Applicant respectfully requests withdrawal of the rejections.

CONCLUSION

Applicant submits the application is in condition for allowance, and an early notice to that effect is requested.

Respectfully submitted,

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